CLAIMS

1. A submount, comprising:

(a) a submount substrate; and

(b) a solder layer that:

(b1) is formed on the top surface of the submount substrate; and

(b2) has a surface roughness, Ra, of at most 0.18 μm before the solder layer is melted.

2. A submount as defined by claim 1, wherein the solder layer has a surface roughness, Ra, of at most 0.15 μm before it is melted.

3. A submount as defined by claim 1, wherein the solder layer has a surface roughness, Ra, of at most 0.10 μm before it is melted.

4. A submount as defined by claim 1, wherein the solder in the solder layer has an average crystal-grain diameter of at most 3.5 μm before it is melted.

5. A submount as defined by claim 1, wherein the top surface of the submount substrate has a surface roughness, Ra, of at most 0.10 μm.

6. A submount as defined by claim 1, the submount further comprising a solder-protecting barrier layer formed between the submount substrate and the solder layer.

7. A submount as defined by claim 6, the submount further comprising an electrode layer formed between the submount substrate and the solder-protecting barrier layer.

8. A submount as defined by claim 7, the submount further comprising between the submount substrate and the solder-protecting barrier layer:

(a) an intimate-contact layer formed such that it makes contact with the top surface of the submount substrate; and

(b) an element diffusion-preventing layer formed on the intimate-contact layer;

the electrode layer being placed on the element diffusion-preventing layer.

9. A submount as defined by claim 8, wherein:

(a) the intimate-contact layer comprises titanium;

(b) the element diffusion-preventing layer comprises platinum;

(c) the electrode layer comprises gold;

(d) the solder-protecting barrier layer comprises platinum; and

(e) the solder layer comprises gold-tin-based solder.

10. A submount as defined by claim 1, wherein the submount substrate comprises an aluminum nitride-sintered body.

11. A semiconductor unit, comprising:

(a) a submount that comprises:

(a1) a submount substrate; and

(a2) a solder layer that:

(a2a) is formed on the top surface of the submount substrate; and

(a2b) has a surface roughness, Ra, of at most 0.18 μm before the solder layer is melted; and

(b) a semiconductor light-emitting device mounted on the solder layer.